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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/160,657	09/25/1998	JOSEPH W. LYDING	22010-135/IL	6611

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EXAMINER

PERKINS, PAMELA E

ART UNIT	PAPER NUMBER
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2822

DATE MAILED: 07/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/160,657	LYDING ET AL.	
	Examiner	Art Unit	
	Pamela E Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 April 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 40,41,47,60-65 and 76-84 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 40,41,47,60-65,79 and 80 is/are allowed.
- 6) ☒ Claim(s) 76-78 and 81-84 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This office action is in response to the filing of the amendment on 19 April 2004.

Claims 40, 41, 47, 60-65 and 76-84 are pending.

Allowable Subject Matter

Claims 40, 41, 47, 60-65, 79 and 80 are allowed.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance: prior art does not anticipate, teach, or suggest an improved semiconductor device including an insulated gate field effect transistor device having a transistor gate, a gate insulator film not exceeding about 55 Angstroms thickness interposed between the transistor and a channel of the transistor device and an interface between a semiconductive silicon layer and a gate insulating film, conductive contacts to a drain, source and on the gate insulating film, and a concentration of deuterium introduced into and remaining within the film resulting from post-fabrication passivation of the interface in a heated, deuterium gas-enriched atmosphere at a temperature above about 200°C, the transistor device susceptible to degradation associated with hot carrier stress, the concentration of deuterium substantially reducing the degradation associated with the hot carrier stress and increasing the resilience of the field effect transistor to hot electron effects during operation, as disclosed in the independent claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 81 and 82 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lisenker in view of Yoshitomi.

Claim 81 reads on a transistor having a gate oxide thickness of less than or equal to about 55 angstroms (5.5nm) in which deuterium has been provided in an amount sufficient to reduce degradation associated with hot carrier stress. Claim 81 does not require post-metal annealing.

Lisenker teaches annealing a MOS gate oxide film with deuterium to add deuterium to the silicon oxide film. Lisenker teaches adding deuterium in a quantity sufficient to increase the ratio of deuterated to hydrogenated bonds to greater than about 99:1 (page 11). Lisenker teaches that where hydrogen is used to remove dangling bonds at the Si/SiO₂ interface in transistor gate oxides (page 2, lines 10-25), substitution of hydrogen with deuterium results in transistors having improved stability, quality, and reliability (page 4, lines 32-34). Lisenker differs from claim 81 by not teaching the thickness of the gate oxide layer and therefore differs from the claimed range of less than 55 angstroms.

Yoshitomi establishes that CMOS FETS having a gate oxide thickness not exceeding 55 angstroms (5.5nm) were well known at the time of applicant's invention.

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Specifically, Yoshitomi teaches growing a gate oxide (271 Fig. 29C) having a thickness of 4nm (40 angstroms) (Yoshitomi; col. 16, lines 30-35). One of ordinary skill in the art would recognize that thinner gate oxides are desirable since they lower the operating voltage of the device. It would have been obvious to one of ordinary skill in the art at the time of the invention to produce a gate oxide thickness of 4nm in the device of Lisenker to scale down the operating voltage.

Claim 82. The gate insulator is silicon oxide as discussed above.

Claims 76-78 and 84 are rejected under 35 U.S.C. 103(a) as being unpatentable over any one of Deal, Paivinen, Taguchi, or Cederbaum in view of Lisenker and Yoshitomi.

Post metal annealing using a hydrogen and nitrogen mixture, otherwise known in the art as forming gas, is a standard procedure that is applied to NMOS devices in the prior art. The following references are listed chronologically as of their filing date (the significance of the chronology will be discussed in conjunction with claims that include a gate oxide thickness limitation).

1) U.S. Pat. No. 4,027,380 ("Deal"). Deal teaches a post-metallization anneal using hydrogen at 300-500°C on a CMOS (both NMOS and PMOS) device (col. 9, lines 33-53). Deal explains that the purpose of the post metal anneal is to minimize the fast interface state density which adversely affects threshold voltages. Filed January 16, 1977.

2) U.S. Pat. No. 4,212,100 ("Paivinen"), Col. 7, lines 5-10. Paivinen teaches post aluminum sintering in forming gas (10% H, 90%N, 5 minutes, 400°C) to provide

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improved metallurgical bonding between the aluminum and the polysilicon portions remaining on the substrate. Paivinen teaches an NMOS device. The gate oxide thickness is 1000 angstroms (col. 6, lines 9-14). Filed September 23, 1977.

3) U.S. Pat. No. 5,198,880 ("Taguchi"), col. 4, lines 39-45. Taguchi teaches post aluminum metallization annealing in forming gas at 450°C after forming CMOS devices (both PMOS and NMOS). The gate oxide thickness is 700 angstroms (col. 3, last paragraph). Continuation of application filed June 19, 1990.

4) U.S. Pat. No. 5,320,975 ("Cederbaum"). Cederbaum teaches post annealing (at any subsequent level) in a forming gas (hydrogen and nitrogen mixture, 400°C for 30 minutes) applied to a CMOS (both PMOS and NMOS) array. Cederbaum explains that hydrogen passivation of dangling bonds is effected by the forming gas anneal. (Cederbaum, paragraph bridging cols. 13-14). The gate oxide thickness is 110nm (100 angstroms) (col. 10, lines 8-10). Filed March 22, 1994.

Lisenker's teaching would motivate one of ordinary skill in the art to replace the hydrogen in the post metal hydrogen anneal in any one of Deal, Paivinen, Taguchi, or Cederbaum with deuterium. Based on Lisenker, one would expect this modification to result in beneficial deuterium being incorporated into the device rather than hydrogen.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the conventional post-metal hydrogen anneal (i.e., any one of Deal, Paivinen, Taguchi, or Cederbaum) to replace the hydrogen with deuterium as suggested by Lisenker. One of ordinary skill in the art would have expected that this

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modification would provide some improvement in sensitivity to hot carrier degradation as taught by Lisenker.

Claim 83 is rejected under 35 U.S.C. 103(a) as being unpatentable over Deal, Paivinen, Taguchi, or Cederbaum in view of Lisenker and Yoshitomi as applied to claim 81 above, and further in view of Hori.

Claim 83 requires a silicon oxynitride gate insulator.

Hori teaches a silicon oxynitride gate insulator being used in place of a silicon oxide gate insulator having the advantage of greater dielectric strength (higher dielectric constant) without sacrificing mobility.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use silicon oxynitride as a gate insulator in the device taught by Deal, Paivinen, Taguchi, or Cederbaum in view of Lisenker to increase the dielectric constant while maintaining sufficient mobility as taught by Hori.

Response to Arguments

Applicant's arguments, filed 19 April 2004, with respect to claims 40, 41, 47, 60-65, 79 and 80 have been fully considered and are persuasive. The rejection of claims 40, 41, 47, 60-65, 79 and 80 has been withdrawn.

Applicant's arguments filed 19 April 2004, with respect to claims 76-78 and 81-84 have been fully considered but they are not persuasive. As stated above, Deal, Paivinen, Taguchi, or Cederbaum in view of Lisenker and Yoshitomi disclose the semiconductor device as described in claims 76 and 81.

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In response to the applicant's arguments, claims 76 and 81 do not disclose a concentration of deuterium introduced into and remaining within the film resulting from post-fabrication passivation of the interface in a heated, deuterium gas-enriched atmosphere.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP



Michael Trinh
Primary Examiner
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